IPB-I2S-TDM-4S
4x I²S/TDM Configurable Serial Audio Transceiver

Overview

The IPB-I2S-TDM-4S core is a serial audio transceiver capable of transmitting and receiving up to four digital audio streams in full-duplex TDM mode.

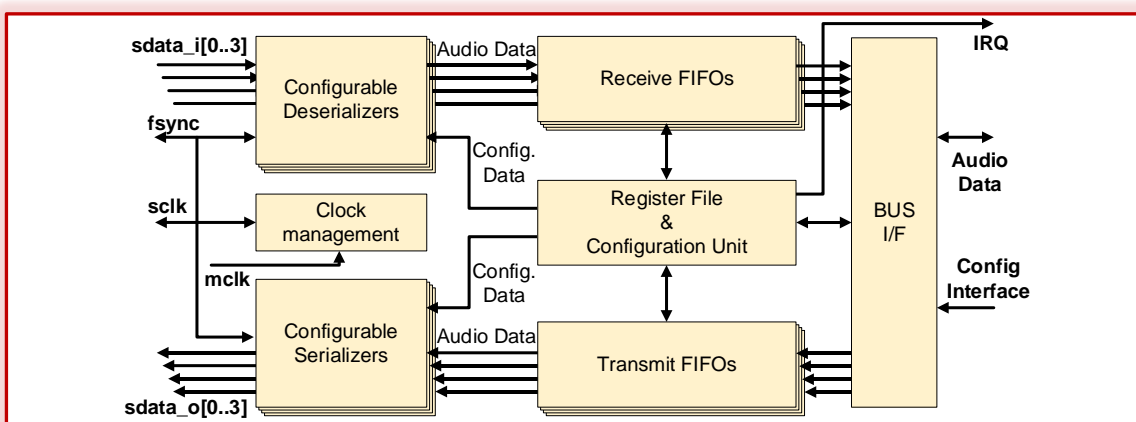IP cores with lower or higher I²S/TDM stream counts are available upon request.

The IPB-I2S-TDM-4S core supports all well-known stereo formats, namely, I²S, Left-Justified or Right-Justified.

The bus interface is available with options including AMBA-AXI, AMBA-AHB, AMBA-APB, or a basic parallel interface.

Deliverables

- Verilog source code or FPGA netlist
- Verilog testbench for RTL simulation
- Datasheet
- Synthesis constraints
- Example software driver in C
- Protected simulation model (for evaluation)
- Time limited FPGA netlist (for evaluation)

Block Diagram

Features

- All I²S/TDM streams share the same audio clocks, but can support different data formats
- Runtime configurable audio formats: multi-channel serial audio (TDM) and also I²S, Left-Justified, and Right-Justified
- Each I²S/TDM stream supports up to 256 audio channels
- Full duplex operation
- Compatible with all sample rates
- Runtime configurable sample width, ranging from 8 to 32 bits per sample
- DMA ready data interface
- Reports FIFO full/empty conditions and number of samples
- Supports audio bus operation in both master and slave modes

Benefits

Enables rapid development of a TDM audio front-end interface compatible with various vendor-specific formats

Disclaimer: IPbloq reserves the right to modify the current technical specifications without notice

Xilinx FPGAs	LUTs	REGs	RAMB18	DSPs
Artix 7 or Spartan 7	2,540	2,300	8	0
Kintex Ultrascale+	2,838	2,562	0	0

Intel FPGAs	ALMs	REGs	RAMs	DSPs
Cyclone 10	1,923	2,459	8	0

ASICs	Gate count	Area (mm²)
TSMC 65 nm	9,700	0,040
Embedded RAMs	Words	Size (bits)
4 x Two Port RAMs	64	33
4 x Two Port RAMs	64	32

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