IPB-AAC-LC-ME-14

14-ES AAC-LC AUDIO ENCODER

Overview

The IPB-AAC-LC-ME-14 is an IP core for encoding up to 14 stereo audio streams in real-time, in one of the following configurations: 14 stereo channels or 12 stereo channels and a 5.1 channel.

The IPB-AAC-LC-ME-14 software requires an audio engine platform named **IPB-PLAT-71**, which includes 7 processors and one accelerator.

The encoder can be configured, run and monitored by means of a configuration, control, and status register file accessed by APB or SPI.

AAC-LC Stereo Features

- AAC-LC encoders are compliant with the ISO/IEC 13818-7, ISO/IEC 14496-3 and Japanese ARIB standard
- Supported channel modes: mono, stereo and dual mono
- Supported sample rates: 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kHz
- Maximum 16-bit input audio resolution
- Minimum latency[(1)]: 1 frame
- Supported transport types: raw, ADIF, LATM/LOAS and ADTS (with ARIB support and CRC)
- Supported bitrate control modes: fixed framing, constant bitrate and variable bitrate

AAC-LC 5.1 Features

- MPEG2/4 AAC-LC are compliant with the ISO/IEC 13818-7, ISO/IEC 14496-3 and Japanese ARIB standard
- Supported channel modes: mono, dual mono, stereo (2.0), 2.1, 3.0, 3.1, 4.0, 5.0, and 5.1
- Supported sampling rates: 8, 16, 22.05, 32, 44, 44.1 and 48 kHz
- Maximum 16-bit input audio resolution
- Minimum latency: 1 frame for up to 2 channels, 2 frames for more than 2 channels per stream
- Supported transport types: raw, ADIF, LATM/LOAS and ADTS (with ARIB support and CRC)
- Supported bitrate control modes: fixed framing, constant bitrate and variable bitrate

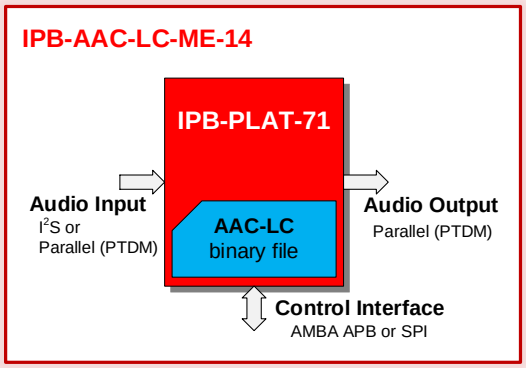
[(1)] The input frame time was not included in this value

[(2)] Latency can be expanded by increasing the size of the output FIFOs

Generic Features

- All encoders use the Fraunhofer IIS software
- Configurable output latency useful to synchronize with other sources (up to 8 frames[(2)])
- Software interface protocol for control, configuration and monitoring
- Parameter change without stopping the encoding process

Block Diagram



Implementation Results

for Xilinx Kintex® UltraScale+™

LUTs	62500	**Block RAM**	479
FFs	31000	**UltraRAM**	44
DSPs	28	**Freq (MHz)**	165

This version does not require any external memory, but other trade-offs are possible to reduce the FPGA memory usage

Deliverables

- Optimized netlist for the target FPGA
- Software manual
- Hardware datasheet
- Synthesis constraints

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