IPB-SPDIF-TX

CONFIGURABLE SPDIF-AES3 TRANSMITTER

Overview

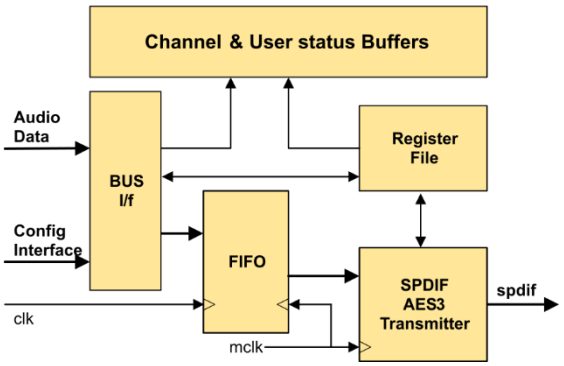
The IPB-SPDIF-TX is a digital audio transmitter supporting the SPDIF (IEC60958) and the AES3 standards for stereo PCM audio transmission, with hardware support for the IEC61937 and SMPTE337M standards for non-PCM multi-channel compressed audio.

The core is very configurable allowing many features of the standards to be supported either by software or hardware.

Deliverables

- Verilog source code or FPGA netlist
- Verilog testbench for RTL simulation
- Synthesis constraints
- Datasheet
- Example software driver

Block Diagram



Features

- Supports the SPDIF (IEC60958) and AES3 standards for stereo PCM audio transmission
- Supports the IEC61937, SMPTE 337M standards for non-PCM audio transmission (Dolby Digital, AAC, DTS, MPEG, etc.)
- Automatic insertion of stuffing bits in non-PCM mode
- Supports any sample rate Fs by setting the audio clock frequency to 256x Fs including 32, 44.1, 48, 96 and 192 kHz
- Programmable FIFO level trigger
- Optional memory mapped buffers for Channel Status and User Bits
- Optional separate interfaces for data and control
- Latency: 0.5/Fs
- Can use clock recovered by the IPB-SPDIF-RX IP core (SPDIF-AES3 receiver)

Implementation results

Xilinx FPGAs	Slices	LUTs	Registers
Spartan-6™	342	513	536
Virtex-6™	206	399	473

ASICs	Cell count
TSMC 45 nm	13320

Benefits

- Choice of backend interface: AMBA APB, AMBA AHB or parallel interface with REQ/ACK handshaking

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