IPB-AAC-LC-MD

AAC-LC AUDIO DECODER

Overview

The **AAC-LC Audio Decoder** (IPB-AAC-LC-MD) is a software IP for decoding up to 6 audio channels in real-time. It is designed to run on our IPB-PLAT audio engine platform.

The IPB-AAC-LC-MD software requires an instance of the IPB-PLAT audio engine platform named **IPB-PLAT-10**. This instance contains only one processor.

The user can upload the IPB-AAC-LC-MD program using a hardware interface. The program can be configured, run and monitored by means of a configuration, control, and status register file, accessed by the same control interface.

The audio input and output interfaces include a native parallel interface. Other interfaces, such as, I²S/TDM and SPDIF/AES3 are also available.

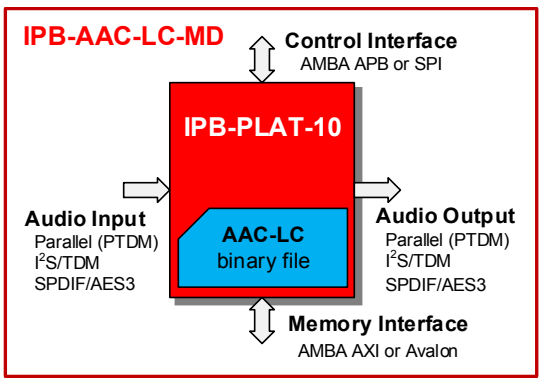
Features

- AAC-LC decoders are compliant with the ISO/IEC 13818-7 audio standard, using Fraunhofer IIS high quality software
- Supported channel modes: mono, dual mono, stereo (2.0), 2.1, 3.0, 3.1, 4.0, 5.0, and 5.1
- Supported sample rates: 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48 kHz
- Supported transport types: ADTS, LATM, and LOAS
- 16-bit output audio resolution
- Requires 1,35 MB of external memory
- Configurable output latency useful to synchronize with other sources (e.g. video)
- Minimum latency: 1 frame assuming burst data input
- Software interface protocol for control, configuration and monitoring
- Parameter change while muting or repeating one frame
- Real time operation @80 MHz for worst-case settings

Benefits

- Low operation frequency
- Low power consumption
- Optimizable to fulfill different design specifications

Block Diagram



Implementation Results(1)

Intel/Altera Cyclone-V

ALMs	Registers	DSPs	Memory bits
4,100	4,080	4	312,000

Xilinx Spartan-6

LUTs	FFs	DSPs	BRAM 18K
6,400	3,550	4	22

(1) Implementation results for other FPGAs or ASIC technologies can be provided upon request

Deliverables

- Program binary
- Software manual
- Hardware datasheet
- RTL or FPGA netlist
- Implementation constraints

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